# Europa Clipper Comprehensive FPGA Risk Reduction

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## Task Overview

The purpose of this document is to provide a detailed task outline for the Europa Clipper (EC) comprehensive FPGA TID/SEE Assurance Solutions Task. This document provides information to assist designers interested in implementation of FPGA devices in EC. Although this work is ongoing, the present document provides an overview of the current effort and indicates the direction being taken to cover all reasonable candidates for use in EC. The document provides a list of selected devices to be tested, known data, and what will be required to complete a down-select based on Electronic Parts Engineering (EPE) requirements.
The high-level objectives and proposed implementation of the task are as follows:

- Objectives:
    - (FY14) Provide EC specific FPGA down-select based on EPE requirements. Remove the guesswork and uncertainty in the selection and application of FPGA's for EC with respect to both radiation and reliability.
    - (Continued work) Develop a tool to aid in the compare and contrast of system (device implementation) level error rates based on FPGA selection.
- Deliverables:
    - (FY14) Report of exhaustive test data on select devices. Initial application guideline and SEEA-ready data. Separate packaging report.
- Proposed Implementation
    - Collect existing SEE and TID data, as available, on select devices. Execute SEE and TID tests on select devices. Packaging to provide white paper study based on manufacturer data only.

## Introduction

When investigating the effects of space radiation on Field Programmable Gate Arrays (FPGA), both Total Ionizing Dose (TID) and Single Event Effects (SEE) must be considered. In CMOS devices, TID causes electron-hole pairs in the gate insulation layers from the total ionizing energy deposited by photons or particles such as electrons, protons or heavy ions. This cumulative effect leads to the degradation of electrical (DC parametrics) and timing parameters at the device, circuit and system levels. Such degradation can eventually lead to complete device failure. Conversely, SEEs in digital devices are caused by high-energy particles traveling through a sensitive volume in the semiconductor and leaving an ionized track behind. Such ionization may lead to destructive [e.g. Single Event Latchup (SEL) or Single Event Dielectric Rupture (SEDR)] or non-destructive events. Non-destructive events may be transient [Single Event Transients (SET)] or stable events, such as Single Event Functional Interrupt (SEFI), Single Event Upset (SEU) or

Multiple Bit Upset (MBU).

In order to obtain an understanding of the radiation response of various FPGA, a high level understanding of the device's architecture must be grasped. Effectively, the manner by which the device is configured, i.e. the underlying technology of the FPGA fabric, determines the radiation response. FPGAs consist of a configurable logical block (CLB) that is placed and routed within the FPGA. The FPGA's configuration determines function and location of that CLB and connection to other CLBs. Each FPGA element (combinatorial logic (CL), Flip-flop (FF), clock, reset, arbitrary signal, etc…) has a set of configurable switches that determines the functionality. There are three primary types of FPGA technologies: SRAM (reconfigurable), Antifuse (OTP), and flash (reconfigurable). Because all of the flash technologies on the market fail at relatively low TID levels [<50krad(Si)], they will not be covered in the document.

Up front, SRAM-based, reprogrammable FPGA devices provide designers with relatively low-cost, low core voltages, and high-speed capability compared to their one-time-programmable (OTP) anti-fuse counterparts. SEU-hardened FPGAs (e.g. OTP anti-fuse devices or RHBD reconfigurable) typically require little to no mitigation efforts by the designer, as they are mitigated for SEE through process or design. However, the speed and re-configurability of SRAM-based FPGAs come at the cost of the need to mitigate against SEU, thereby reducing speed and increasing design complexity and power.

For reconfigurable SRAM-based FPGAS, configuration bit upsets are the dominant upset mode of the device, other effects such as Digital SET or SEU of flip-flops are typically ignored (save for RHBD SRAM such as the V5QV). A per-bit cross-section versus effective Linear Energy Transfer (LET) curve is first developed for the configuration cell upset susceptibility from heavy ions; see Figure 1 (Allen & Swift, Virtex-4QV Static SEU Characterization Summary, 2008). In addition to the heavy ion cross-section plot, proton susceptibility is measured and described with a per-bit cross-section versus proton energy (MeV) plot. From this data, a per-bit SEU rate

can be developed for any given space environment.

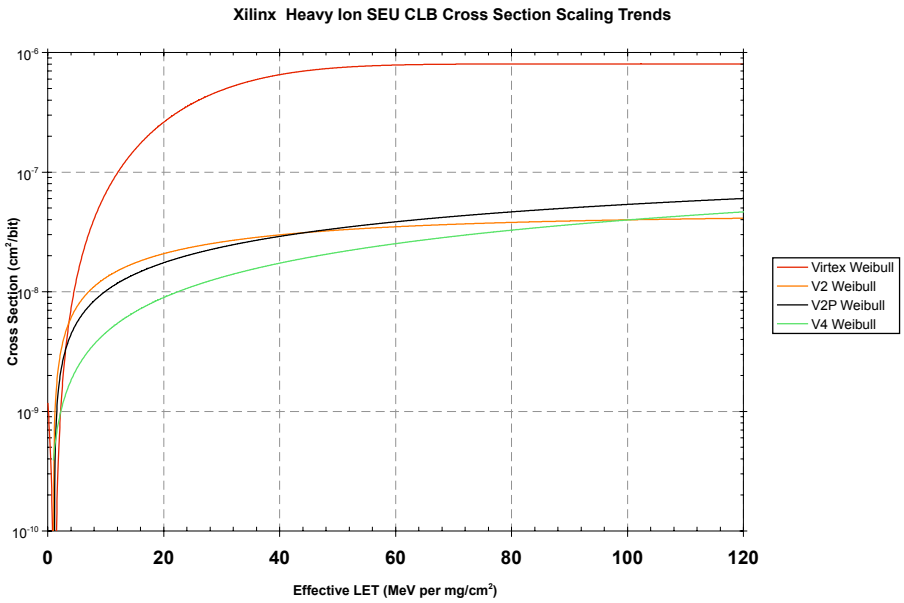


**Figure 1 Per-bit cross-sections versus effective LET for four Virtex families of FPGA: Virtex. Virtex-II, Virtex-II Pro, and Virtex-4.**

Once a per-bit cross-section is established, resource utilization must be determined in order to approximate a system level error rate, i.e. not every configuration SEU will cause a given design to fail. To further illustrate the point, 60% to 70% of the configuration bits in a typical device are routing bits. Of those bits, a typical ratio of bits not affecting a design to those affecting a design is between 9:1 and 4:1 (Tseng, 2009). That being said, estimating the number of configuration bits that will affect a design if upset is not as straightforward as using the post place and route "device utilization summary" report from the development toolset. While using utilization reports will provide resource use percentages, they don't include routing bits and will provide a gross underestimate. However, there are a few other, more accurate options. A more accurate option is the use of fault injection to estimate the bitstream susceptibility to upset. Finally, the most accurate, yet most costly, method by which to quantify FPGA utilization is to perform accelerator testing. By developing a system-error (per device) versus effective LET cross-section, one can accurately quantify the number of configuration bits affecting the design. Yet, because design mitigation is typically an iterative process, already expensive accelerator testing can quickly become cost prohibitive. While there are a handful of ways to estimate the number of bits that will affect a design, the designer and/or mission assurance engineer must understand how that number was quantified and what that means to the overall system rate.

For OTP antifuse devices, the configuration is determined by creating an electrically conductive path in metal layers of the FPGA. Once the configuration is set, there is no changing it, but the antifuse technology does have the advantage of not being

susceptible to SEU. However, SETs do occur in combinatorial logic and can get clocked into registers to generate an erroneous state. There is therefore an inherent frequency dependence in the SEE data which must be taken into account when acquiring SEE response data, reviewing data of others, or applying that data to an application; see Figure 2 below.

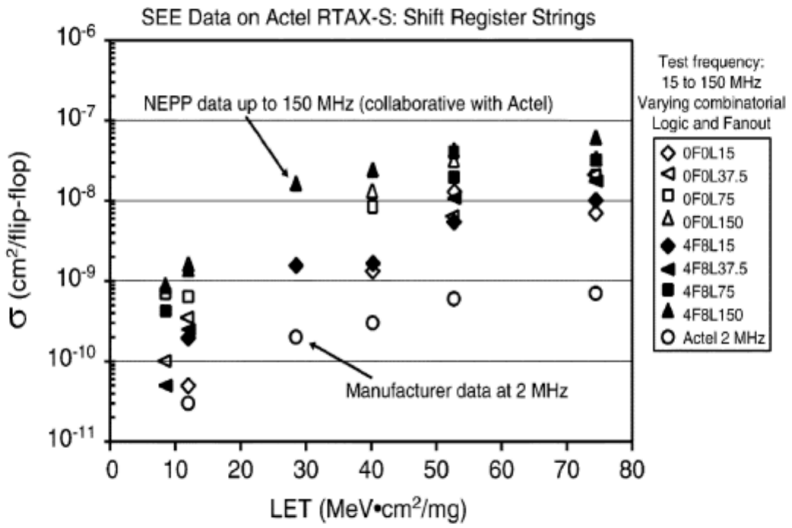


**Figure 2 Per-flip-flop cross-sections versus effective LET for various test structures at various frequencies.**

# Selected Devices

We have proposed testing of FPGAs from two different manufacturers: Microsemi (formerly Actel), and Xilinx. The stringent total ionizing dose (TID) requirements limit the potential candidates. A few additional candidates from Aeroflex and Atmel have recently been targeted due to requests from the JPL design community for smaller, low power FPGAs. An overview of available data for the various test candidates is as follows:

## Xilinx Virtex-4

### TID

No known TID testing has been performed on the commercial Virtex-4 FPGA. However, because the mask of the V4 and V4QV are exactly the same, it is assumed the TID limit of the commercial device is the same as the Mil/Aero version. The assumed TID tolerance of the device is 300krad(Si). The task will perform a quick TID test to confirm the assumption.

### SEE

The radiation susceptibility of the commercial Xilinx Virtex-4 (V4) family of devices was well characterized in (George, Koga, Swift, & Allen, 2006). The SEE characterization of the configuration bitstream due to both proton and heavy ion irradiation was completely characterized, and correlate well to the Virtex-4 QV (V4QV) devices. While in depth characterization of SEFI modes were not performed on the V4, again, due to the same mask sets, the SEFI response from the V4QV is applicable. The device is completely SEL immune.

### Packaging and Reliability

The die is equivalent to the V4QV, save it being on bulk substrate instead of a thin epitaxial layer. It is a cheaper COTS solution to the V4QV, with more options with regards to resources, i.e. an engineer could procure any of the devices, where the V4QV parts are limited to 4 specific parts. However, being COTS would require packaging related up screening. Both NASA Electronic Part and Packaging (NEPP) tasks and the FY15 Europa Clipper FPGA task are looking into package qualification for this device.

## Xilinx Virtex-4 QV

### TID

The reported TID limit is 300krad(Si); the actual failure level is most likely higher.

### SEE

The V4QV device was extremely well characterized for both protons and heavy ions (Allen & Swift, Virtex-4QV Static SEU Characterization Summary, 2008), and is SEL immune. The static SEE characterization includes characterizations of SEFI modes. A second round of testing thoroughly investigated dynamic and mitigated testing of IP (Allen, Virtex-4QV Dynamic and Mitigated Single Event Upset Characterization Report, 2009).

### Packaging and Reliability

The device is available in a ceramic flip-chip column grid array. The process still requires JPL qualification. Both NASA Electronic Part and Packaging (NEPP) tasks and the FY15 Europa Clipper FPGA task are looking into package qualification for this device.

## Xilinx Virtex-5

### TID

While no TID testing has been performed on the V5 devices, TID testing performed on test structures showed no degradation past 500krad(Si).

### SEE

The commercial Virtex-5 (V5) devices do have some static heavy ion and proton characterization data available (Quinn, Morgan, Graham, Krone, & Caffrey, 2007), however, most of the radiation testing for this technology node was performed on the Virtex-5QV (V5QV). Unlike the Virtex-4 technology node, no comparison can be

made between the QV and COTS devices, as the QV was completely redesigned for RHBD. That being said, there are several advantages to keeping V5 on the table: Firstly, and obviously, cost. Beyond the financial aspect, V5FX130T and V5QV are footprint compatible, allowing a designer to leave either option open in the early design/tradeoff phase. V5 has several options within the technology node, allowing for more flexibility in with regards to power and resource options.

#### Packaging and Reliability

Packaging is the same as V4, FCBGA RoHS, and needs to be studied (a subject of the FY15 FPGA task).

### Xilinx Virtex-5 QV

#### TID

The TID levels for this device are reported to be 1Mrad(Si), the reality is that it is closer to 4Mrad(Si).

#### SEE

The radiation tolerance of the Xilinx Virtex-5QV device is well known (Swift & Allen, Virtex-5QV Static SEU Characterization Summary, 2013) (Swift & Allen, Virtex 5-QV Architectural Features SEU Summary Report, 2013). The device is SEL immune and effectively flight ready with regards to SEE susceptibility.

#### Packaging and Reliability

The primary concern with the device, again, is the packaging (to be covered in the FY15 EC FPGA task).

### Xilinx Virtex-7 (Includes Zynq, Kintex, and Artix)

The Xilinx Virtex-7 is the latest state-of-the-art device from Xilinx. The primary draw for selecting this device is the lower power and high speeds the part is capable of. That being said, unlike all of the other devices, this part's radiation response was completely unknown prior to this task.

#### TID

No TID testing has been performed on this device. However, due to the technology node (28nm), the TID failure level is expected to be above 500krad(Si).

#### SEE

Limited SEE testing has been performed on both the Zynq and the Kintex devices. The configuration, embedded RAM and flip-flops have been characterized as function of heavy ion LET. However, a high current mode was observed in both test campaigns. The current could either be caused by a SEFI mode or by single-event latchup. If it is determined that it is the latter, it would prohibit the use of these devices for Europa Clipper.

#### Packaging and Reliability

Packaging is the same as V4 and V5, FCBGA RoHS, and needs to be studied (a subject of the FY15 FPGA task).

### Microsemi RTAX2000/RTAX4000

#### TID

The devices have a TID tolerance up to 200krad(Si) parametric and 300krad(Si) functional. The parametric failure is the IDD going over the specified datasheet limit, which may be acceptable in some applications. We feel we can extend the TID limit further by testing at a lower dose rate and by applying a dose profile where by the device is irradiated and annealed with a mission specific dose profile.

#### SEE

Microsemi's (formerly Actel), RTAX devices are SEL immune, have a relatively low, well-defined SEE susceptibility (Microsemi Corp.).

#### Packaging and Reliability

Packaging is not a concern unlike the Xilinx devices as the package is available in Mil-Std-883 Class B and QML Class V qualified land grid array or ceramic column grid array packages.

## Other Device Candidates

### Aeroflex UT6325

The Aeroflex UT6325 RadTol Eclipse FPGA is a one-time-programmable (OTP), relatively small, low power, lower speed (120MHz) device. It is specified to 300krad(Si) and is SEL immune with relatively low single event susceptibility. The device is both QML Q and QML V qualified.

### Atmel AT40KEL040

Built on a 0.35um process, the device is older and slower (60MHz internal performance), but is specified to a TID level of 300krad(Si) and is SEL immune. Available with QML-Q or –V qualifications, the device is SRAM based and therefore reprogrammable. The configuration memory and associated logic have been hardened to increase the SEE tolerance of the device.

### Atmel ATF280E

Built on a 0.18um process, this device is also relatively slow (50MHz internal performance), but is also specified to a TID level of 300krad(Si) and is SEL immune. Available with QML-Q or –V qualifications, the device is SRAM based and therefore reprogrammable. The configuration memory and associated logic have been hardened to increase the SEE tolerance of the device.