# A Novel Asynchronous Integrating Latching (NAIL) controller for MEMS deformable mirrors

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# Contents

# 4 Objective

This whitepaper sets forth the planned Strategic Astrophysical Technology (SAT) milestones for the project entitled the Novel Asynchronous Integrating Latching (NAIL) controller for Microelectromechanical systems (MEMS) deformable mirrors (DMs). It documents those project milestones and the metrics and success criteria for their evaluation.

Simply put, the goals of this project are to develop a controller for a Boston Micromachines Corp (BMC) kilo-DM (952 actuators) with performance requirements needed to support a mission like the Planetary Imaging Concept Testbed Using a Recoverable Experiment (PICTURE) series of missions [Mendillo et al., 2012, Chakrabarti et al., 2016, Cook et al., 2015, Mendillo et al., 2023]. We have selected this level requirement as the minimum meaningful requirements for a useful controller. Those requirements are enumerated in section 7. We will remain cognizant of the more stringent requirements for the Habitable Worlds Observatory (HWO) and will ensure that there is a development path to those requirements for future extensions of this work. This effort is not intended to greatly improve the performance of the state of the art controller but rather to reduce the size, weight, and power (SWAP) of existing controllers to make a more practical flight system. This new architecture is also amenable to extensions to higher performance in the future.

# 5 Introduction

The various internal exoplanet coronagraph concepts [e.g. Mennesson et al., 2003, Guyon et al., 2006, Kasdin et al., 2005] are designed to detect planets with star-planet high contrast ratios. Some of this can be accounted for by the Airy fall off of the point spread function (PSF) and more than another order of magnitude can be subtracted by differencing images at different roll angles (called angular differential imaging (ADI)). Lafrenière et al. [2009] have shown that optimal processing of multiple images can suppress the PSF at a level of about 1 percent. Similarly, Ford et al. [2003] find that PSF subtraction reduces the residual PSF of the HST Advanced Camera for Surveys (ACS) by about a factor of 100. Less germane but still illuminating is a study by Destree and Snow [2009] which quantifies the Space Telescope Imaging Spectrograph (STIS) fixed pattern noise at a few percent of the continuum.

Nonetheless, this leaves a large fraction of starlight which must be suppressed by the coronagraph. This, in turn, implies that the wavefront must be smooth (on the spatial scales which correspond to the star-planet angular separation) at a level well beyond the state of the art for simple polished optics. Such optics might conceivably, at great cost, meet $\lambda/10^{1.5}$. Higher wavefront quality in a multi element system is simply not possible with polished glass. To meet these requirements designers have specified some sort of DM to "clean up" the wavefront. For a system operating at 5000Å this implies control of the DM to between 1 and 100 Å in surface position depending on the coronagraph requirements and design [Kenworthy and Haffert, 2025].

This requirement is somewhat modified by techniques which do not simply flatten the wavefront but rather tailor the wavefront to create a "dark hole" in the image at the location

of the desired observation [e.g. Give'on et al., 2007]. The requirements for HWO are not final but required precisions as low as 10 pm have been suggested.

There are many different DMs in use. These include piezoelectric actuators [e.g. Bendek et al., 2018], voice coil actuators [e.g. Berdeu et al., 2023] and electrostatic MEMS mirrors [e.g. Potier et al., 2023]. It is the last that is of interest here. These DMs are in common use and under consideration for use in the HWO [Crill, 2023]. They are intrinsically very low power, high precision, large format (i.e. high pixel count) devices and are thus well suited to space based applications.

## 5.1 State of the Art

As discussed in section 5, despite the proliferation of coronagraph designs and operational schemes, they are all limited in there contrast by our ability to shape and control the wavefront. Different coronagraphs and operational schemes will shape the wavefront differently but the physical limit of the contrast being proportional to the square of the wavefront error is a simple physical limit for all systems [Ryan et al., 2013].

The state-of-the-art ten years ago for a controller to support a BMC 1000 actuator DM (a kilo-DM) was a 4 inch tall unit designed to be mounted in a standard 18U rack and connected to the DM through a series of flex cables. The unit drew several 10s of watts and achieved 14 bit resolution.

Bendek et al. [2016] developed a small controller suitable for space applications. That controller used significantly less size, and weight than previous systems and was small enough that it could be located with the DM on the optical bench.

Unfortunately, this results in a heat load (the controller power) of $\sim 10$ Watts into the optical bench. Furthermore, the Bendek controller depends on amplifier chips which are no longer in production. As a result, this controller can no longer be produced.

Previous controllers are amplifier based and are limited by the bandwidth-voltage-power constraints of those amplifiers. NAIL, the controller described here, is charge based. By metering charge into the actuators NAIL only applies power as needed to move the actuator and thus operates much more efficiently at much lower power.

More recently Haughwout et al. [2023] have developed a commercial-off-the-shelf (COTS) based driver for risk tolerant missions. The detailed power requirements for this design are not reported but based on the general architecture an estimate of 10 to 20 watts seems reasonable.

The Cambridge Innovations controller (https://www.camb-innov.com/) uses similar technology to these systems and has similar SWAP characteristics.

## 5.2 Summary

DMs are a ubiquitous tool for ground based observatories and they are starting to be used in the civil space program. The key bar to further adoption is the control electronics. For small satellite missions the large SWAP of the controllers is prohibitive. For larger missions the

high power ($\sim$ 10 watts) leaked into the optical system (if the controller is proximate to the DM ) or the extensive cabling (if the controller is not) complicates the thermal design and adds risk of a harness failure [Douglas et al., 2016] and the general weight and complexity of a large harness. In large missions risks associated with not damaging the thousands of fine wires in the harness become even more pronounced. NAIL will enable or mitigate risk in missions and their associated new science ranging from small satellites to the HWO.

# 6 Implementation Plan

The broad outlines of our implementation plan are:

1. Prepare the Application Specific Integrated Circuit (ASIC) level design and simulation in-house at University of Massachusetts Lowell (UML) in consultation with the ASIC vendor.

2. Pass that design to the ASIC vendor for physical layout, mask fabrication, wafer fabrication, and prototype assembly into a functional device.

3. Test the prototype at UML in-house for basic functionality, performance, and environmental robustness.

We have been working with the ASIC vendor MinDCet[1] in the development of this proposal and plan to use them for the eventual ASIC procurement. Other vendors are available should the need arise, mitigating the risk of having a single procurement channel.

## 6.1 Current Status

We have developed a low-fidelity prototype of the NAIL controller, called the Single-channel Novel Asynchronous Integrating Latching (SNAIL) (see Figure 4) and used it to demonstrate the basic functionality of NAIL. [Bailey et al., 2025 submitted] We thus estimate that we are currently at TRL 4. We have used the prototype to inform and validate our performance calculations. While in those calculations we have used the characteristics measured in the low-fidelity prototype, we expect the final ASIC implementation to have better performance and thus our calculations represent a pessimistic performance estimate.

We are currently fabricating a next generation prototype, Quad-channel Asynchronous Integrating Latching (QUAIL), which will be used to test further design details and to investigate issues such as cross talk.

## 6.2 Basic design

The NAIL ASIC operates a MEMS electrostatic actuator DM produced by BMC. The DM consists of a face sheet and an array of actuators (see Figure 1). The face sheet may be

[1] https://www.mindcet.com/

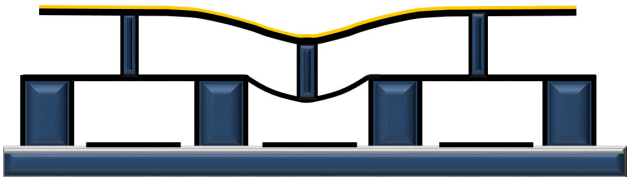


Figure 1: A MEMS DM is a capacitive device. Charge is injected onto an electrode at the bottom of the device which creates am electric field which in turn pulls the actuator down and reflective face sheet down. The capacitance of the actuator represents the physical limit to the actuator performance. This figure is from https://bostonmicromachines.com/-products/deformable-mirrors/standard-deformable-mirrors/

a continuous membrane or it may be cut (segmented) into tiles each covering one or more actuators. The facesheet is attached to the actuators by posts attached to the top of the actuators.

The actuator consists of an electrode "floor" on the lower surface, a box of rigid walls, and a flexible "roof". The floor electrode and and the roof form a parallel plate capacitor with $\sim 200$ pF capacitance. As charge is applied to the electrode an electric field is created between the electrode and the roof. This exerts a force on the roof and causes it to deflect, pulling on the post which, in turn, deforms the upper membrane. The membrane is metallized and acts as a mirror.

NAIL precisely controls the charge on the actuator electrodes in order to position and shape the membrane. In operation it will receive pixel addresses and data values over a serial line from the control electronics (usually a control computer). An I/O module within the ASIC will set the address on the mux to access the desired pixel control line. Each pixel will have two such control lines, one to raise the pixel and one to lower it (see Figure 2). This is the integrating aspect of the NAIL control system. Charge is added or removed from the charge already in the actuator. The power applied to the pixel is only the power to move the pixel from its previous position to its next one. Since most actuator commands in operation are for very slight adjustments in position, these commands take very little power.

After addressing the correct line, the I/O module will send the data value to the selected pulse generator. The generator will form a pulse whose width is proportional to the data value. This pulse will inject charge into or drain charge out of the desired pixel (see Figure 3). NAIL is asynchronous in that any pixel can be commanded at any time in any order. As a result, unused pixels need not be addressed and will draw no charge and no power.

### 6.2.1 Pulse generator and resolution

A key novelty of this design is using the pulse width of an individual pulse to control the step size of an individual pixel. By reducing the charge injection problem to a pulse timing problem we use the very high precision and dynamic range of electronic timing circuits. The minimum size of the charge packet injected into the actuator is set by the $RC$ time of the charging circuit and the minimum switching time of the transistor. With moderately slow

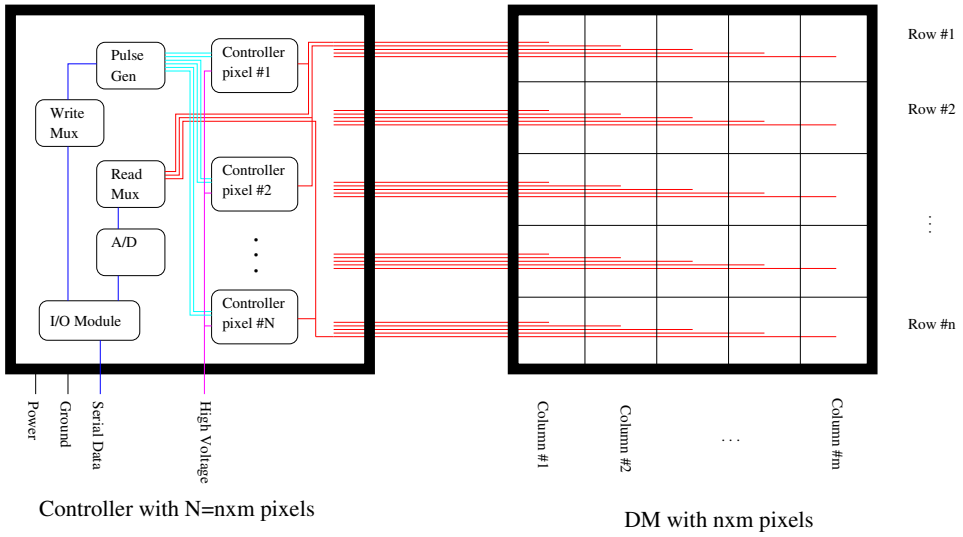



Figure 2: The controller described here, NAIL, (left) is small enough to share a printed circuit board with the DM. It can mitigate the significant cabling difficulties of larger controllers.

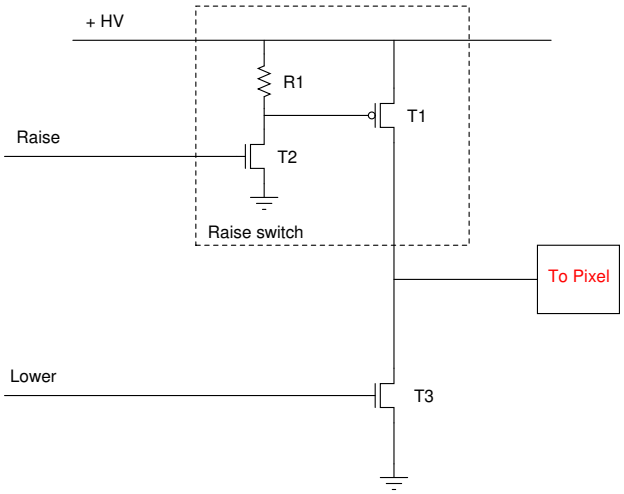



Figure 3: The pixel control circuit uses paired N and P type HV CMOS gates to pulse charge into and out of an individual pixel. These transistors operate with a high (typically 200V) potential between the source and drain requiring a high voltage ASIC.

discrete power transistors our low-fidelity prototype was able to demonstrate a Least Significant Bit (LSB) step size of 0.045 nm. These transistors were selected for their availability rather than their performance so an optimized system will have much better performance. The first NAIL ASIC will be developed with 16 bit precision. Since this is fundamentally a timing circuit higher precision is easily possible.

The pulse width is set by a counter. The desired width is written into the counter and its output remains high while the counter counts down. The counters are clocked by a precision oscillator. Drift in this oscillator will result in gain changes in the controller but high stability oscillators are common so we do not anticipate this being a significant source of error.

For a given transistor switching speed, a higher $RC$ time constant gives more precise actuator positioning. A key modeling task in this effort will be to understand the details of the ASIC foundry process in order to optimize the high voltage transistor switching time with the internal resistance of the high voltage line ($R$) and the output capacitance of the ASIC ($C$). We can optimize both $R$ and $C$ to achieve the best precision and ripple characteristics given the transistor properties. The transistor properties are a function of both the fabrication process and the detailed layout/design and will not be known until the design firm is under contract and the fabrication house selected.

### 6.2.2 Pixel control circuit

The pixel control circuit is a key novelty in this design. It uses paired N and P type HV Field Effect Transistors (FETs) to pulse charge into and out of an individual pixel in order to step it up and down (see Figure 3). By pulsing the charge in, the only power used is that actually needed to move the pixel; if the system is quiescent no power is used.

### 6.2.3 Optimizing precision and ripple

When an actuator is not addressed the raising and lowering transistors are off and the actuator is isolated. During this time there is a small leakage current which slowly drains charge from the actuator causing the pixel to sag. This leakage is a result of the leakage current of the transistor and surface currents through any contamination on either the controller board or the DM itself. The amount of sag is related to the leakage current by the output capacitance of the controller.

In operation each pixel will need to be periodically refreshed to maintain position. Our tests show that the leakage current of an isolated BMC Multi-DM actuator connected to the prototype controller board results in a displacement loss of 63.2% every 1,950 seconds, returning to 0 nm after 162.5 minutes. If each pixel is refreshed at a rate of 10 Hz, this would result in an output jitter of 0.005% of the target displacement, maintaining $> 1 : 2^{15}$ actuator positioning accuracy (of SNAIL). The optimized transistors of NAIL will have lower leakage currents and lower ripple than SNAIL. This ripple can be further reduced by increasing the output capacitance of the controller. The increase can be accomplished either in chip or with small capacitors external to the device. Larger output capacitance results in lower ripple and higher power draw.

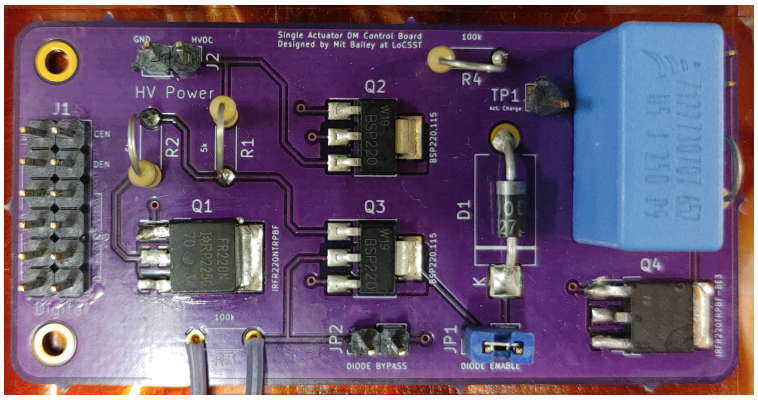



Figure 4: This low-fidelity prototype has been used to demonstrate NAIL's basic functionality (see Figure 5) and validate our performance predictions(see Figure 6). The prototype uses a few transistors to operate a single channel. By implementing NAIL as an ASIC we can easily accommodate the several thousand transistors needed to run a full sized DM in a single chip.

### 6.3 Development Plan

The NAIL prototype (see Figure 4) was developed by graduate student Mitchell Bailey at UML. He will be deeply involved in developing the NAIL ASIC. With the assistance of the rest of the UML team he will prepare the necessary schematics and other documents and will tune the design to maximize the system performance given the detailed constraints of the silicon fabrication foundry. These schematics will be passed to our outside vendor (nominally MinDCet) to create the masks and other fabrication documentation. The vendor will then have the ASIC fabricated, package it for use, and deliver it to UML. UML will be responsible for functional testing, environmental testing, and demonstrating the device in use.

We plan to implement two rounds of design, fabrication, and test in this three year effort. The first round will implement the basic design described in Section 6.2. It will allow us to test our understanding and modeling of the smaller scale implementation of NAIL. It is possible, but unlikely, that we will meet all of the milestones described in Section 7.2 with the first run. We will then use the results of our first effort to refine our performance models and implement any corrections or improvements required. We will then implement a second round which will result in a TRL 5 device.

## 7 Milestone definition

The NAIL program will have one performance milestone and 14 schedule milestones.

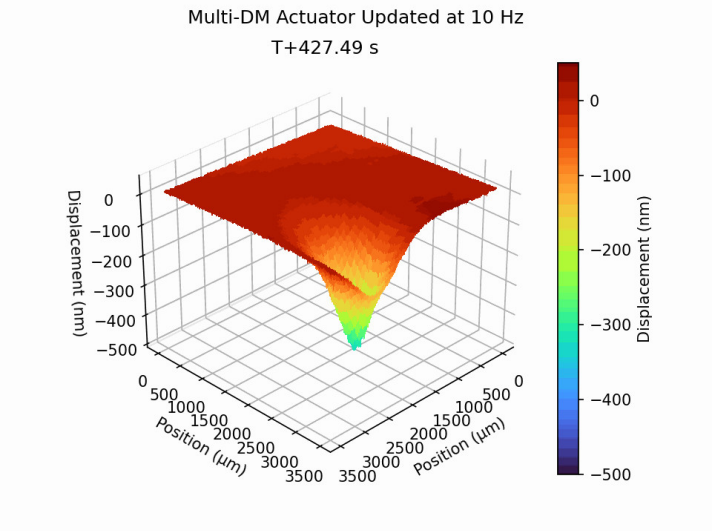



Figure 5: We have use the low-fidelity SNAIL prototype to demonstrate the functionality of the controller and to validate out calculations of power consumption. Here we show optical measurements of the surface as we slowly increase the charge on an actuator using the low-fidelity SNAIL prototype.

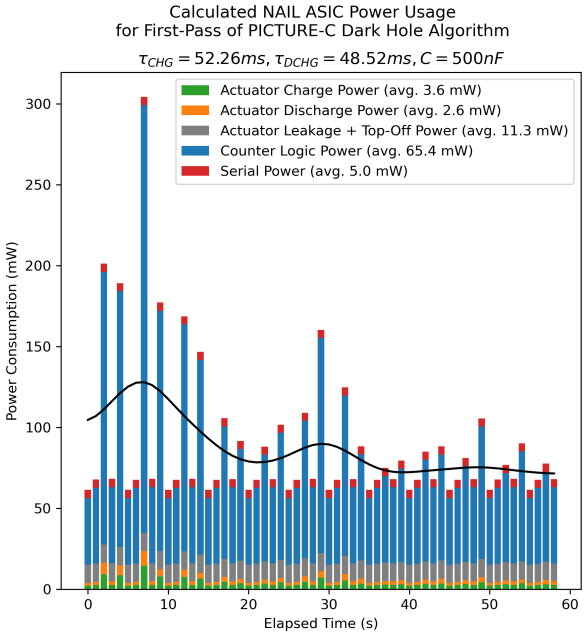



Figure 6: We have simulated the performance of NAIL in flight by modeling its response to the as-sent in-flight commanding of the *PICTURE C* DM. These calculations indicate that had NAIL been available for *PICTURE C* the controller would have drawn several hundred milliwatts rather than the $\sim 10$ watts actually dissipated by the controller. As the algorithm runs, the necessary corrections decrease in magnitude thereby further lowering the power.

## 7.1 Performance milestone

The performance milestones for NAIL all relate to its ability to control a BMC DM at a useful level with a low SWAP. We have flowed this down to the following functional requirements and goals.

This project will meet its first and only performance milestone when we have demonstrated a controller which meets these requirements.

**Actuator count** NAIL shall control a full BMC kilo-DM. A BMC kilo-DM will have 952 actuators. Our goal is to do this in a single ASIC. Our requirement shall be to do this in one or more ASICs and other components which can be accommodated on a $90 \times 96$ mm board.

**Power** NAIL shall operate at less than 1 watt with a goal of 250 mW (see figure 6).

**Resolution** NAIL shall be capable of controlling the position of each actuator to less than 0.1 nm measured over long time scales.

This will result in a phase accuracy of $\lambda/5000$ with 1000 nm light. The design shall not preclude future improvements to control to less than 0.01 nm. For reference, 0.1 nm corresponds to $2^{13.88}$ precision at 1.5 $\mu$ stroke full range. Our goal is to produce a controller capable of 16 bit precision and resolution and our requirement is to produce a controller with slightly worse than 14 bit precision and resolution. We anticipate that one bit at 16 bit resolution corresponds to $2.2 \times 10^{-16}$ coulombs of charge into the actuator. Using the Bendek controller [Bendek et al., 2020] with 14 bit accuracy Potier et al. [2023] achieved $< 10^{-7}$ contrast.

**Ripple** NAIL shall be capable of controlling the position of each actuator so that the RMS deviation over time of each actuator is less than $\pm 1$ nm.

**Range** NAIL shall be able to control each actuator from 0 volts to 90% of the full voltage of the high voltage rail.

**Bandwidth** Space applications are comparatively slow and there is no practical requirement on the bandwidth of this device. Any reasonable architecture will be considerably faster than the sensors required to detect the wavefront and update the DM solution. NAIL's goal is to operate all actuators at $\geq 100$ Hz. Since the actuators move asynchronously, the actuators move independently, only the actuators which need to move need to be addressed, and the data rates are considerably faster than the actuator motion times for all but the smallest motions, this rate is largely independent of the number of pixels on the DM.

**Interface** NAIL shall be controlled via a USB 2 or USB 3 interface. Digital power and return shall be via the same interface. High voltage and high voltage return shall be via a high voltage connection.

## 7.2 Schedule milestones

Each design revision will be developed through a series of seven milestone reviews.

**Kick off** A kick off meeting will be held as soon as the MindCet procurement is in place.

**Concept review** A concept review will be held approximately 2 months after kickoff. In this meeting the functional block diagrams and system architecture will be finalized. Approximately 20% to 40% of the schematic design will be complete

**Final design review** A final design review will be held approximately 5 months after kick-off. At this review the complete schematic for the system will be approved.

**Critical design review** A critical design review will be held approximately 8 months after kickoff. The final layout will be approved and fabrication will be authorized.

**Design delivery** The design will be delivered to the foundry approximately 9 months after kickoff.

**Packaging start** The device will return from the foundry approximately 12 months after kickoff and packaging at MindCet will begin.

**Delivery to UML** The device will be delivered to UML approximately 16 months after kickoff.

# 8 Measurements and data analysis

While it is possible to make direct electrical measurements of the charge on the controller, the capacitance of the DM pixel is a significant factor in the performance of the controller and thus those measurements are of limited value. As a result, NAIL will be tested at UML using multi- and kilo-DMs. The BMC DMs come in a range of sizes. The smallest, least expensive, have about 140 actuators and are referred to as multi-DMs. The kilo-DMs have about 1000 actuators, and the newest largest DMs are the K+ DMs with about 2000 actuators. See https://bostonmicromachines.com/products/deformable-mirrors-/standard-deformable-mirrors/ for details). These systems all operate with the same technology, the significant differences are simply cost, actuator count, and pixel size. We will use the less capable, low cost multi-DMs for our initial tests and the larger kilo-DMs for our final testing. The DM control accuracy and resolution will be measured with UML's PhaseCam 6110 from 4D Instruments[1]. The PhaseCam 6110 captures surface deflection images multiple times per second at an optimal RMS of $6.328 \pm 0.3164$ nm precision using a 632.8 nm laser.

[1] https://4dtechnology.com/

## 8.1 Actuator position resolution

In order to establish a resolution of 0.1 nm/analog to digital unit (ADU) with a PhaseCam with an error of $\sim 0.3$ nm we will need to average repeated measurements of the displacement. This will be done in two ways. First, we will command a single pixel repeatedly one step forward and measure the position at each step. By measuring the slope of the response we can demonstrate the resolution of a single step. Next, we repeatedly ground the entire DM to bring it to a known state and then command it to a pattern. By repeatedly measuring the pattern we can establish the precision to which the DM is moving to more precision than any one measurement or any one pixel.

## 8.2 Power

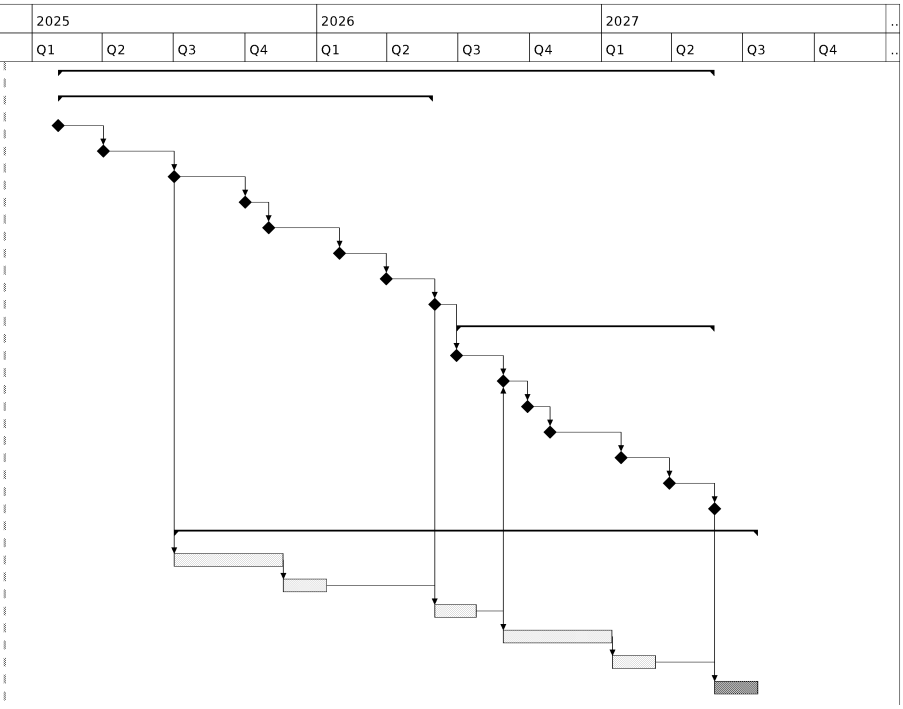
Power (voltage and current) will be measured via ordinary laboratory equipment.

## 8.3 Equipment availability

The PhaseCam is located in the LOwell Center for Space Science and Technology (LoCSST) labs and is used by the LoCSST faculty on their various projects. This is primarily Co-Is Chakrabarti and Mendillo. It will be shared between this program, Planetary Imaging Concept Testbed Using a Recoverable Experiment - Debris Disk (PICTURE-D), and any other projects which may arise. Its scheduling is entirely under the control of the PI and Co-Is allowing straightforward resolution of any scheduling conflicts.

# 9 Schedule

| Name | Work |
|---|---|
| **MindCet Milestones** | |
| **Revision 1** | |
| Kick Off | |
| Concept Review | |
| Final Design Review 1 | |
| Critical Design Review 1 | |
| Design delivery/tapeout 1 | |
| Packaging start 1 | |
| Characterization and test 1 | |
| Delivery to UML 1 | |
| **Revision 2** | |
| Start design 2 | |
| Final Design Review 2 | |
| Critical Design Review 2 | |
| Design delivery/tapeout 2 | |
| Packaging start 2 | |
| Characterization and test 2 | |
| Delivery to UML 2 | |
| **UML effort** | **360d** |
| Rev 1 simulation | 100d |
| Test 1 setup | 40d |
| Rev 1 testing | 40d |
| Rev 2 simulation | 100d |
| Test 2 setup | 40d |
| Rev 2 testing | 40d |




A significant fraction of this work is being carried out by the design firm MindCet. As a result the schedule is paced by the formal interactions between UML and MindCet. The project allows for 2 design cycles and each design cycle steps through these pacing reviews as listed in section 7.2.

Testing at UML will then proceed. The results of the testing will be compared to simulations and the results published. A kickoff for the second design cycle will be initiated after the first delivery and the second fabrication will proceed with similar timing.

# References


Mitchell Bailey, Timothy Cook, Sunip Mukherjee, Kuravi Hewawasam, Christopher B. Mendillo, and Supriya Chakrabarti. Efficient precision control of MEMS deformable mirrors. *Journal of Astronomical Telescopes, Instruments, and Systems*, 2025 submitted.

Eduardo Bendek, Dana Lynch, Eugene Pluzhnik, Ruslan Belikov, Benjamin Klamm, Elizabeth Hyde, and Katherine Mumm. Development of a miniaturized deformable mirror controller. In Enrico Marchetti, Laird M. Close, and Jean-Pierre Véran, editors, *Adaptive Optics Systems V*, volume 9909 of *Society of Photo-Optical Instrumentation Engineers (SPIE) Conference Series*, page 990984, July 2016. doi: 10.1117/12.2233929.

Eduardo Bendek, Ruslan Belikov, Dan Sirbu, Stuart B. Shaklan, and A. J. Eldorado Riggs. Enabling Super-Nyquist Wavefront Control on WFIRST. In *American Astronomical*

*Society Meeting Abstracts #231*, volume 231 of *American Astronomical Society Meeting Abstracts*, page 402.07, January 2018.

Eduardo Bendek, Garreth Ruane, Camilo Mejia Prada, Christopher B. Mendillo, A. J. Eldorado Riggs, and Eugene Serabyn. Microelectromechanical deformable mirror development for high-contrast imaging, part 1: miniaturized, flight-capable control electronics. *Journal of Astronomical Telescopes, Instruments, and Systems*, 6:045001, October 2020. doi: 10.1117/1.JATIS.6.4.045001.

Anthony Berdeu, Michel Tallon, Éric Thiébaut, and Maud Langlois. Analytical modelling of adaptive optics systems: Role of the influence function. *A&A*, 674:A112, June 2023. doi: 10.1051/0004-6361/202245327.

S. Chakrabarti, C. B. Mendillo, T. A. Cook, J. F. Martel, S. C. Finn, G. A. Howe, K. Hewawasam, and E. S. Douglas. Planet Imaging Coronagraphic Technology Using a Reconfigurable Experimental Base (PICTURE-B): The Second in the Series of Suborbital Exoplanet Experiments. *Journal of Astronomical Instrumentation*, 5: 1640004-595, March 2016. doi: 10.1142/S2251171716400043.

T. Cook, K. Cahoy, S. Chakrabarti, E. Douglas, S. C. Finn, M. Kuchner, N. Lewis, A. Marinan, J. Martel, D. Mawet, B. Mazin, S. R. Meeker, C. Mendillo, G. Serabyn, D. Stuchlik, and M. Swain. Planetary Imaging Concept Testbed Using a Recoverable Experiment-Coronagraph (PICTURE C). *Journal of Astronomical Telescopes, Instruments, and Systems*, 1(4):044001, October 2015. doi: 10.1117/1.JATIS.1.4.044001.

Brendan Crill. Progress in Technology for Exoplanet Missions: An appendix to the NASA Exoplanet Exploration Program Technology Plan. https://exoplanets.nasa.gov/internal_resources/2595/, January 2023.

J. D. Destree and T. P. Snow. Unidentified Features in the Ultraviolet Spectrum of X Per. *ApJ*, 697:684–692, May 2009. doi: 10.1088/0004-637X/697/1/684.

E. S. Douglas, C. B. Mendillo, T. A. Cook, and S. Chakrabarti. Wavefront sensing in space from the PICTURE-B sounding rocket. In *Society of Photo-Optical Instrumentation Engineers (SPIE) Conference Series*, volume 9904 of *Proc SPIE*, page 99046A, July 2016. doi: 10.1117/12.2235631.

H. C. Ford, M. Clampin, G. F. Hartig, G. D. Illingworth, M. Sirianni, A. R. Martel, G. R. Meurer, W. J. McCann, P. C. Sullivan, F. Bartko, N. Benitez, J. Blakeslee, R. Bouwens, T. Broadhurst, R. A. Brown, C. J. Burrows, D. Campbell, E. S. Cheng, P. D. Feldman, M. Franx, D. A. Golimowski, C. Gronwall, R. A. Kimble, J. E. Krist, M. P. Lesser, D. Magee, G. Miley, M. Postman, M. D. Rafal, P. Rosati, W. B. Sparks, H. D. Tran, Z. I. Tsvetanov, P. Volmer, R. L. White, and R. A. Woodruff. Overview of the Advanced Camera for Surveys on-orbit performance. In *Society of Photo-Optical Instrumentation*

*Engineers (SPIE) Conference Series*, volume 4854, pages 81–94, February 2003. doi: 10.1117/12.460040.

A. Give'on, B. Kern, S. Shaklan, D. C. Moody, and L. Pueyo. Broadband wavefront correction algorithm for high-contrast imaging systems. In *Society of Photo-Optical Instrumentation Engineers (SPIE) Conference Series*, volume 6691, September 2007. doi: 10.1117/12.733122.

O. Guyon, E. A. Pluzhnik, M. J. Kuchner, B. Collins, and S. T. Ridgway. Theoretical Limits on Extrasolar Terrestrial Planet Detection with Coronagraphs. *ApJS*, 167:81–99, November 2006. doi: 10.1086/507630.

Christian Haughwout, Kyle Van Gorkom, Stephen Kaye, Kerri Cahoy, Daewook Kim, and Ewan S. Douglas. Compact deformable mirror driver electronics for risk tolerant astrophysics missions. In Tony B. Hull, Daewook Kim, and Pascal Hallibert, editors, *Society of Photo-Optical Instrumentation Engineers (SPIE) Conference Series*, volume 12677 of *Society of Photo-Optical Instrumentation Engineers (SPIE) Conference Series*, page 1267706, October 2023. doi: 10.1117/12.2677714.

N. Jeremy Kasdin, Robert J. Vanderbei, Michael G. Littman, and David N. Spergel. Optimal one-dimensional apodizations and shaped pupils for planet finding coronagraphy. *Ap Opt*, 44(7):1117–1128, 2005. URL `http://ao.osa.org/abstract.cfm?URI=ao-44-7-1117`.

Matthew A. Kenworthy and Sebastiaan Y. Haffert. High-contrast coronagraphy. *Annual Review of Astronomy and Astrophysics*, 2025. ISSN 0066-4146. doi: https://doi.org/10.1146/annurev-astro-021225-022840. URL `https://www.annualreviews.org/content/journals/10.1146/annurev-astro-021225-022840`.

D. Lafrenière, C. Marois, R. Doyon, and T. Barman. HST/NICMOS Detection of HR 8799 b in 1998. *ApJL*, 694:L148–L152, April 2009. doi: 10.1088/0004-637X/694/2/L148.

C. B. Mendillo, B. A. Hicks, T. A. Cook, T. G. Bifano, D. A. Content, B. F. Lane, B. M. Levine, D. Rabin, S. R. Rao, R. Samuele, E. Schmidtlin, M. Shao, J. K. Wallace, and S. Chakrabarti. PICTURE: a sounding rocket experiment for direct imaging of an extrasolar planetary environment. In *Society of Photo-Optical Instrumentation Engineers (SPIE) Conference Series*, volume 8442, September 2012. doi: 10.1117/12.926408.

Christopher B. Mendillo, Kuravi Hewawasam, Jason Martel, Thaddeus Potter, Sunip Mukherjee, Timothy A. Cook, Supriya Chakrabarti, Frans Snik, David S. Doelman, Dan Sirbu, Ruslan Belikov, Eduardo Bendek, Karl Stapelfeldt, and Schuyler Grace Wolff. The PICTURE-C exoplanetary imaging balloon mission: second flight results and the transition to a new mission, PICTURE-D. In *Society of Photo-Optical Instrumentation Engineers (SPIE) Conference Series*, volume 12680 of *Society of Photo-Optical*

*Instrumentation Engineers (SPIE) Conference Series*, page 126800F, October 2023. doi: 10.1117/12.2677518.

B. P. Mennesson, M. Shao, B. M. Levine, J. K. Wallace, D. T. Liu, E. Serabyn, S. C. Unwin, and C. A. Beichman. Optical Planet Discoverer: how to turn a 1.5-m class space telescope into a powerful exo-planetary systems imager. In A. B. Schultz, editor, *Society of Photo-Optical Instrumentation Engineers (SPIE) Conference Series*, volume 4860, pages 32–44, February 2003.

Axel Potier, Camilo Mejia Prada, Garreth Ruane, Hong Tang, Wesley Baxter, Duncan Liu, A. J. Eldorado Riggs, Phillip K. Poon, Eduardo Bendek, Nick Siegler, Mary Soria, Mark Hetzel, Charlie Lam, and Paul Bierden. Random vibration testing of microelectromechanical deformable mirrors for space-based high-contrast imaging. *Journal of Astronomical Telescopes, Instruments, and Systems*, 9:029001, April 2023. doi: 10.1117/1.JATIS.9.2.029001.

Peter J. Ryan, Steven A. Cornelissen, Charlie V. Lam, and Paul A. Bierden. Performance analysis of two high actuator count MEMS deformable mirrors. In Scot S. Olivier, Thomas G. Bifano, and Joel Kubby, editors, *MEMS Adaptive Optics VII*, volume 8617 of *Society of Photo-Optical Instrumentation Engineers (SPIE) Conference Series*, page 861705, March 2013. doi: 10.1117/12.2005299.

# List of Acronyms

**ACS** HST Advanced Camera for Surveys

**ADI** angular differential imaging

**ADU** analog to digital unit

**ASIC** Application Specific Integrated Circuit

**BMC** Boston Micromachines Corp

**COTS** commercial-off-the-shelf

**DM** deformable mirror

**FET** Field Effect Transistor

**HV** High Voltage

**HWO** Habitable Worlds Observatory

**LoCSST** LOwell Center for Space Science and Technology

**LSB** Least Significant Bit

**MEMS** Microelectromechanical systems

**NAIL** Novel Asynchronous Integrating Latching

**PICTURE** Planetary Imaging Concept Testbed Using a Recoverable Experiment

**PICTURE-D** Planetary Imaging Concept Testbed Using a Recoverable Experiment - Debris Disk

**PSF** point spread function

**QUAIL** Quad-channel Asynchronous Integrating Latching

**SAT** Strategic Astrophysical Technology

**SNAIL** Single-channel Novel Asynchronous Integrating Latching

**STIS** Space Telescope Imaging Spectrograph

**SWAP** size, weight, and power

**UML** University of Massachusetts Lowell